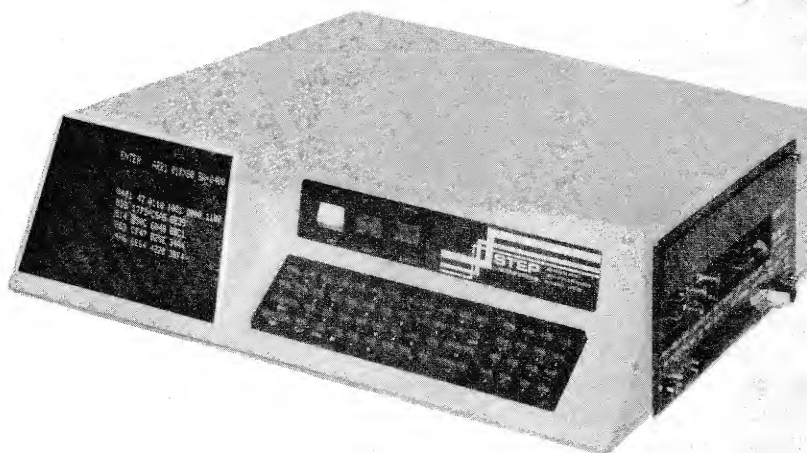


STEP
ENGINEERING

STEP-2 FITS

FIRMWARE INTEGRATION TEST STATION



A new concept in microcode development, test, and debug, featuring:

- Up to 768K bits of high-speed storage in one or two independent arrays.
- Reconfigurable memory organization from 8 to 96 bits per word.
- Real time, in-system operation.
- Total application/processor independency and transparency.
- Real-time system monitoring and diagnostic capability.
- Interactive English-language commands.
- Powerful word-oriented editor.
- Multiple memory load and dump options.
- ROM Simulation for quick system connect
- Compatible with existing software base.
- Full software support.

DESCRIPTION

STEP-2, Firmware Integration and Test Station (FITS), is a flexible instrument for firmware testing, firmware integration and system testing of microcoded processors and controllers. It provides:

A reconfigurable, variable word width, Writable Control Store for *real-time* firmware emulation.

Diagnostic instrumentation for following and analyzing the path of execution of the processor/controller under development.

A sophisticated word-oriented editor for "close to the hardware" system fault isolation and program patches.

A method of loading and dumping programs from and to external computers and PROM programmers.

The instrument is completely independent of and transparent to the system under development, requiring no special control lines or interconnects.

Powerful English-language commands along with extensive description messages make the system easy to use and work with. All commands and data are entered through the alphanumeric and hex keypads with the results displayed on the CRT.

WRITABLE CONTROL STORE

The Writable Control Store, WCS, simulates all or part of the microcode/application memory in *real time* during system development. It provides the ability to rapidly change program contents permitting fast and efficient checkout and generation of processor and system functions. Up to three Writable Control Stores organized as one or two independent arrays, can be resident in STEP-2. Six Writable Control Stores are possible with optional Expansion Chassis. The WCS comes in two varieties: a 32K bit version which can be organized 1Kx32, 2Kx16 or 4Kx8, and a 128K bit version with 4Kx32 or 8Kx16 organization. System organizations 8 to 96 bits per word in four bit increments can be efficiently achieved; 192 bits per word are possible if two arrays are concatenated. The unique ability to simulate more than one memory array allows STEP-2 to be useful in multiprocessor systems, systems with ROM address mapping, and systems with separate microcode and application memories.

SYSTEM INTERCONNECT

The easiest and most convenient way of connecting STEP-2 to the target processor is through ROM Simulation modules. They plug directly into existing PROM sockets on both breadboard and production systems. Seventeen module types emulate existing ROMs and PROMs mechanically, electrically and functionally and can be field upgraded as PROM types change. The WCS can also be connected directly to the target processor through a ribbon cable array connector. Each WCS has a bit mapping area and choice of interface type (buffered, non-buffered and register) to simplify interconnect.

EDITOR

A word oriented machine code editor simplifies the task of modifying program code to find or correct a problem. Four consecutive memory locations are displayed on the CRT along with a binary representation of the data at the current cursor location. Through the use of the cursor controls, data may be entered at any position within the displayed field, and the current memory locations may be incremented, decremented or scrolled. A block of data may be moved in memory to insert instructions or save a subroutine prior to modification. Individual instructions containing a specified data pattern composed of ones, zeros and don't cares can be located in memory, simplifying the task of modifying output routines or references to specific memory addresses.

DIAGNOSTIC INSTRUMENTATION

Several diagnostic features are incorporated in STEP-2 to enable rapid system debug and test. On each Writable Control Store, a real time breakpoint is provided which can be used to halt the user's processor or trigger a logic analyzer or oscilloscope. The state of each breakpoint along with the current processor address is displayed on the CRT. Multiple breakpoints simplify conditional jump analysis by displaying the alternative program paths being executed. Keyboard functions RUN, HALT, STEP, CYCLE and RESET as well as a halt on breakpoint feature pro-

vide an easy means of controlling the processor during debug. Instruments equipped with the Trace option have a delay counter and combinatorial trace triggers to provide easy specification of trace conditions. The Trace option stores 250 locations in real time allowing reconstruction of the processor's path of execution.

SOFTWARE COMPATIBILITY

STEP-2 acts like a terminal, connecting to computers, mini-computers, development systems, and timesharing systems. Through keyboard control, baud rate and parity are configured to match an existing computer system (or PROM programmer). Once the computer link has been established, files, source code, object code, etc. can be displayed on STEP-2's CRT, or object code can be downloaded into memory. Transfer of object code to or from the external device is automatically initiated and synchronized on operator command.

Two formats are provided for object code transfer, MICROWORDTM and GENPROMTM. The MICROWORDTM format is a word oriented, memory image format which contains address, object code and checksum for each line of code. GENPROMTM is a block transfer mode containing 4 or 8 bit data from successive memory addresses as PROM images. Header, frame and end character are programmable making it easy to interface to any assembler with a PROM output format.

SOFTWARE SUPPORT

For designers who need an assembler, STEP's TMA, Transportable Meta Assembler, can be used for any microprogrammed processor. The TMA is fully compatible with AMDASM and can be installed on most 16 bit (or larger) computers with Fortran and on INTEL® Development Systems. The TMA consists of a Definition Program for entry of op codes, bit fields and symbols, a two pass Assembly Program, and a Formatter Program for outputting object code in either MICROWORDTM or PROM format. Cross reference tables, error listings, source and object code are provided as outputs.

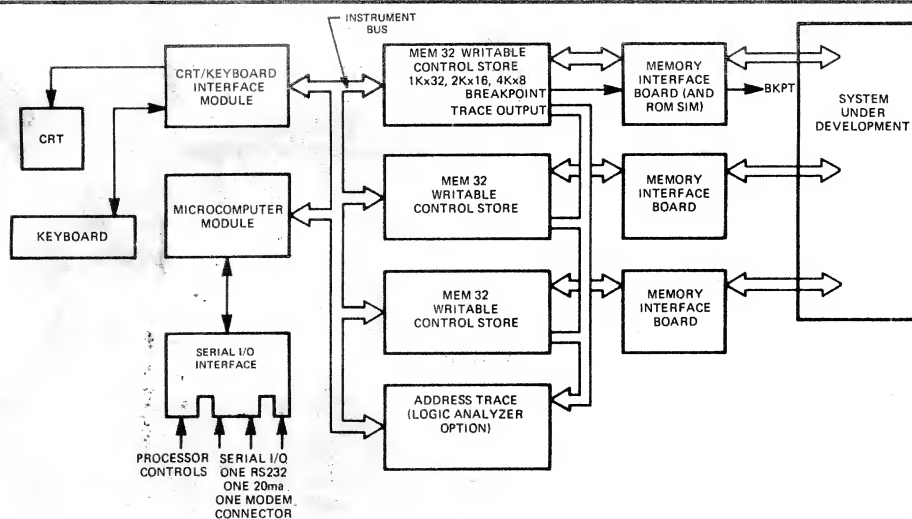
OPERATION

The instrument is controlled through the keyboard and front panel switches. Special purpose function keys simplify editing, downloading and controlling the target processor. An easy-to-read, fully formatted CRT displays memory contents, system states and all information required to operate the instrument. Descriptive error messages reveal improper instrument set-up, invalid commands or addressing, and serial link failures. Recovery from an error condition is automatic upon entering the corrected information. Instrument operation is easy to learn and understand, with training time taking less than a day.

COMMAND SUMMARY

Once the instrument parameters have been specified through SETUP, the commands can be accessed in any order.

CLASS	COMMAND	PARAMETERS (SUBCOMMANDS)	DESCRIPTION
SETUP <i>Specifies instrument parameters</i>	<u>SETUP</u>	NUMBER OF ARRAYS = 1, 2 DATA FORMAT = HEX, OCTAL STARTING ADDR = { FOR ARRAY WIDTH = { EACH ARRAY DEPTH = { ARRAY	Configures the instrument to match the requirements of the target processor. Checks for a memory array specification consistent with the number and organization of the Writable Control Stores.
	<u>ARRAY</u>	ARRAY = 1, 2	Sets memory array to be accessed.
INPUT/OUTPUT <i>Permits communication over serial links with external devices such as computers, PROM programmers, etc.</i>	<u>LOAD</u> <u>DUMP</u> , <u>COMPARE</u> , <u>PUNCH</u>	FORMAT = 0 thru 3 DEVICE = 0 thru 5 START ADDR = NO. OF WORDS = WIDTH } PROM at a time POSITION } formats only (BAUD RATE) (PARITY) (STOP BITS) (HEADER, FRAME, END CHAR) (TEXT) (XPARAM)	LOAD loads object memory in a MICROWORD™ (word at a time) format or one of several PROM formats. Device specifies serial link (20 ma, RS 232, or Modem input as well as line protocol). DUMP dumps the contents of the specified memory array segment over the serial links in PROM or MICROWORD™ image. COMPARE compares the contents of memory to the information being received over the serial link. The address if any location whose contents do not match the incoming data is shown in an error message. PUNCH dumps the contents of the specified memory array segment in PROM BPNF format. (Port 0 only).
	<u>TEXT</u>		When in TEXT, the instrument acts like a limited terminal. TEXT enables easy interface to computers, printers, PROM Programmers, etc.
EDITOR <i>Enables the user to examine or modify memory array contents through the keyboard</i>	<u>ENTER</u>	(ADDRESS) (cursor ↑ ↓ → ←) (QUIT) (CLEAR) (DEL) (C&H) (ENTER)	Enters, modifies or displays data words of up to 96 bits in octal or hex format. Cursor controls permit data to be entered at any position within the four displayed memory locations and allows the currently displayed address to be incremented/decremented or scrolled. The address and bit position of the cursor is displayed along with a binary representation of the data.
	<u>FILL</u>	START ADDR = END ADDR = WORD CONSTANT =	Fills a memory block with a specified word. When no word is specified, the default case is zeros.
MONITOR <i>Real time simulation of processor memory and control/display of processor activity</i>	<u>MOVE</u>	DESTINATION ADDR = START ADDR = NUMBER OF LOCATIONS =	Moves a block of code of at least one word from one memory location to another. The original data remains intact unless written over by the MOVE command.
	<u>SEARCH</u>	START ADDR = END ADDR = COMPARISON WORD = DON'T CARE WORD =	Searches a block of code for a particular data pattern composed of ones, zeros, and don't cares. When a match is found, the address and memory word is displayed and the search is stopped until continued by the operator.
	<u>MONITOR</u>	(BREAKPOINT NO. =) (BRKPT ADDR =) (RUN) (HALT) (STEP) (CYCLE) (PULSE) (EXCHANGE) (QUIT)	Enables the Writable Control Stores and displays breakpoint address and status and current address from user's system. Breakpoints can be modified without effecting processor operation. Control over the processor is provided through the RUN, HALT, STEP, CYCLE and PULSE (RESET) commands.



FUNCTIONAL BLOCK DIAGRAM (ROM emulator outputs not shown.)

SPECIFICATIONS: MODEL STEP-2

ELECTRICAL

Power Supply	100-130 Vac @ 47-440 Hz
Fuse	2.5 amp Slo-Blow

MECHANICAL

	(Table top or rack mounting)
Height	5.25 inches
Width	17.65 inches
Depth	20.0 inches

ENVIRONMENTAL

Operating	0 to 45°C; 0 to 90% relative humidity
Storage	-40 to 85°C; 0 to 95% relative humidity

CRT

Dimensions	5 inches measured diagonally
Viewing Area	13 sq. inches
Display	8 lines by 32 characters/line
Character Size	0.25 x 0.12 inches

KEYBOARD

Dimensions	8.5 inches by 2.3 inches
Keys	Hex Keypad 16
	Special Purpose 8
	Alphanumeric 36
	60 Total

SERIAL INTERFACES

Baud Rate	Individually programmable with data rates of 2400, 1200, 300, 150 or 110 baud. For faster baud rate consult factory.
Stop Bits	1 or 2, individually programmable.
Parity	0; 1, EVEN, ODD
Number	One 20ma current loop, two EIA RS232 compatible, one with modem controls.
Operating Mode	Full or half duplex.

CARD CAGE

Six-slot card cage with three slots committed for instrument functions and options. Three slots available for Writable Control Stores such as MEM 32.

CONTROLS

ON-OFF, RESET, WRITE PROTECT.

STEP-2 OPTIONS

STEP-2E

Expansion Chassis. Adds an additional six slot card cage with power supply in a self-contained enclosure. Three slots are available for additional memory, two for instrument options.

STEP-2R

Rack mounting kit. Enables STEP-2 to be mounted in a standard 19 inch rack.

STEP-2T

Trace option. Provides logic analyzer capabilities. Includes combinatorial breakpoint triggering, delayed trigger and 250 word depth. Refer to the STEP-2T data sheet for further details.

TMA

Transportable Meta Assembler. The Meta Assembler is compatible with AMDASM and can be installed on any 16 bit (or larger) computer with Fortran or an INTEL® Development System. Refer to the TMA data sheet for further details.

MEM 32

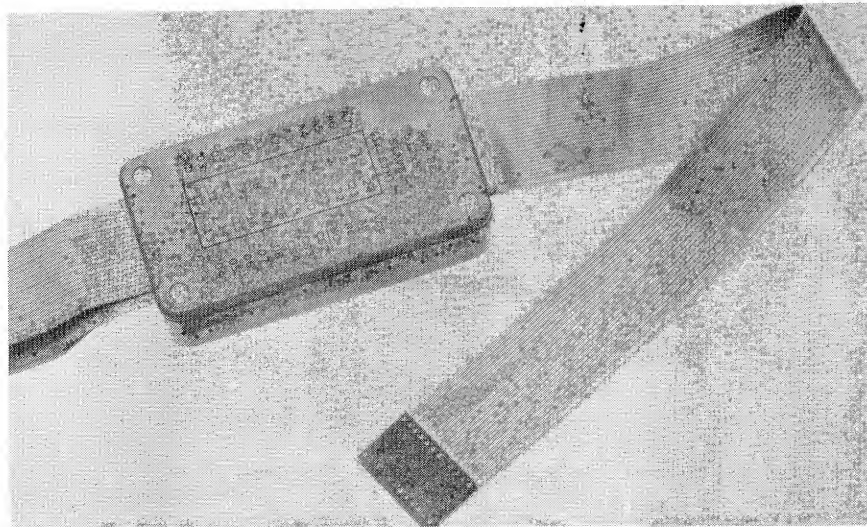
Writable Control Store with 32K bit memory capacity, reconfigurable width and 70ns worst case access time. Refer to the MEM 128 data sheet for further details.

ROM 4/8

ROM simulator plug-ins. Seventeen field upgradable versions simulate over 200 ROMs and PROMs on the market. Refer to the ROM 4/8 data sheet for further details.

STEP ENGINEERING

ROM SIMULATION



FEATURES

- Allows STEP-2 to plug into processor ROM sockets.
- Seventeen types emulate over 200 ROMs and PROMs.
- Directly compatible with MEM-32 Writable Control Store.
- Allows full address space of MEM-32 to be utilized.
- Low Capacitance inputs and output.
- Field Upgradable.

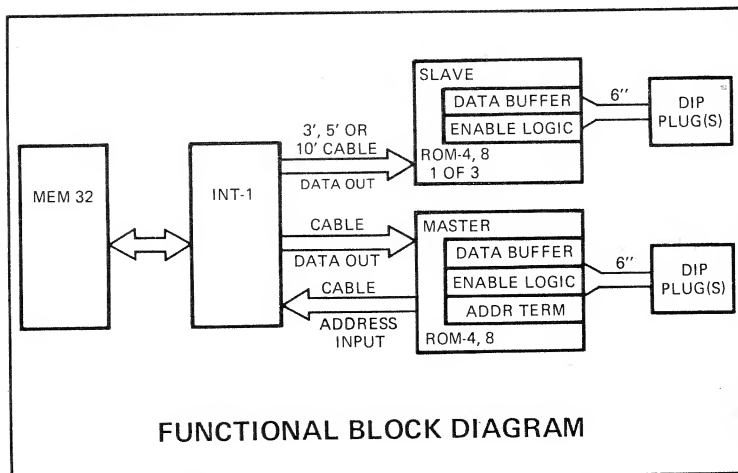
DESCRIPTION

ROM-4/8 are ROM emulation options which give STEP-2 the ability to interface to an existing processor system through its ROM sockets. The outputs of ROM-4/8 are dual-in-line plugs wired to emulate the ROM or PROM of the system's program store. They are designed to interface to MEM-32 Writable Control Stores by plugging into the INT-1 option.

Four ROM-4/8 modules are required for a complete interface to MEM-32. One module, designated MASTER, contains both address inputs and data outputs. The other three, SLAVES, contain just the data outputs. Modules which emulate ROMs with less than 1K address space have external address inputs to allow the full 1K address space of MEM-32 to be utilized. ROM modules can be ORed in the same fashion as ROMs and PROMs through the use of the Chip Select, CS, inputs.

ROM-4 is a series of dual, 4-bit output ROM emulation modules with 16 and 18 pin outputs. It can emulate ROMs with 256x4, 512x4, 1Kx4, and 2Kx4 organizations. ROM-8 is a series of 8-bit output ROM emulation modules with 256x8, 512x8, 1Kx8 and 2Kx8 organizations. Both 20 and 24 pin options are available as well as versions with latching and register outputs.

High reliability is maintained by using a custom, etched, flexible circuit which serves as the interconnect cable between the ROM socket and buffer module. The cable design ensures low crosstalk and reduces input and output capacitance to that of the ROM array being replaced.



ROM-8 SIMULATION

ROM 8A
256x8
MASTER

A3	1	24	Vcc
A4	2	23	A2
A5	3	22	A1
A6	4	21	A0
A7	5	20	CS1
A8	6	19	CS2
01	7	18	STB
02	8	17	08
03	9	16	07
04	10	15	06
11	14	05	
GND	12	13	

AB,A9: AUX INPUT

ROM 8A
256x8
SLAVE

1	24	Vcc
2	23	
3	22	
4	21	
5	20	CS1
6	19	CS2
7	18	STB
8	17	08
9	16	07
10	15	06
11	14	05
GND	12	13

AB,A9: AUX INPUT

ROM 8B
256x8
MASTER

A7	1	24	Vcc
A6	2	23	A8
A5	3	22	
A4	4	21	CS1
A3	5	20	CS2
A2	6	19	CS3
A1	7	18	CS4
A0	8	17	08
01	9	16	07
02	10	15	06
03	11	14	05
GND	12	13	04

AB,A9: AUX INPUT

ROM 8B		
256x8		
SLAVE		
1	24	Vcc
2	23	
3	22	
4	21	CS1
5	20	CS2
6	19	CS3
7	18	CS4
8	17	08
01 9	16	07
02 10	15	06
03 11	14	05
GND 12	13	04

AB,A9: AUX INPUT

ROM 8C
256x8
MASTER

A0	1	20	Vcc
A1	2	19	A7
A2	3	18	A6
A3	4	17	A5
A4	5	16	
01	6	15	CS1
02	7	14	08
03	8	13	07
04	9	12	06
GND	10	11	05

AB,A9: AUX INPUT

ROM 8C
256x8
SLAVE

1	20	Vcc
2	19	
3	18	
4	17	
5	16	
6	15	CS1
7	14	08
8	13	07
9	12	06
10	11	05

AB,A9: AUX INPUT

ROM 8D
512x8
MASTER

A3	1	24	Vcc
A4	2	23	A2
A5	3	22	A1
A6	4	21	A0
A7	5	20	CS1
A8	6	19	CS2
01	7	18	STB
02	8	17	08
03	9	16	07
04	10	15	06
11	14	05	
GND	12	13	

A9: AUX INPUT

ROM 8D
512x8
SLAVE

1	24	Vcc
2	23	
3	22	
4	21	
5	20	CS1
6	19	CS2
7	18	STB
8	17	08
9	16	07
10	15	06
11	14	05
GND	12	13

A9: AUX INPUT

ROM 8E
512x8
MASTER

A7	1	24	Vcc
A6	2	23	A8
A5	3	22	
A4	4	21	CS1
A3	5	20	CS2
A2	6	19	CS3
A1	7	18	CS4
A0	8	17	08
01	9	16	07
02	10	15	06
03	11	14	05
GND	12	13	04

A9: AUX INPUT

ROM 8E
512x8
SLAVE

1	24	Vcc	
2	23		
3	22		
4	21	CS1	
5	20	CS2	
6	19	CS3	
7	18	CS4	
8	17	08	
9	16	07	
02	15	06	
03	14	05	
GND	12	13	04

A9: AUX INPUT

ROM 8F
512x8
MASTER

A0	1	20	Vcc
A1	2	19	A8
A2	3	18	A7
A3	4	17	A6
A4	5	16	A5
01	6	15	CS
02	7	14	08
03	8	13	07
04	9	12	06
GND	10	11	05

A9: AUX INPUT

ROM 8F
512x8
SLAVE

1	20	Vcc
2	19	
3	18	
4	17	
5	16	
6	15	CS
7	14	08
8	13	07
9	12	06
10	11	05

A9: AUX INPUT

ROM 8G
1Kx8
MASTER

A7	1	24	Vcc
A6	2	23	A8
A5	3	22	A9
A4	4	21	CS1
A3	5	20	CS2
A2	6	19	CS3
A1	7	18	CS4
A0	8	17	08
01	9	16	07
02	10	15	06
03	11	14	05
GND	12	13	04

ROM 8G
1Kx8
SLAVE

1	24	Vcc
2	23	
3	22	
4	21	CS1
5	20	CS2
6	19	CS3
7	18	CS4
8	17	08
9	16	07
10	15	06
11	14	05
12	13	04

ROM 8H
1Kx8
MASTER

A7	1	24	Vcc
A6	2	23	A8
A5	3	22	A9
A4	4	21	
A3	5	20	CS
A2	6	19	
A1	7	18	
A0	8	17	08
01	9	16	07
02	10	15	06
03	11	14	05
GND	12	13	04

ROM 8H
1Kx8
SLAVE

1	24	Vcc
2	23	
3	22	
4	21	
5	20	CS
6	19	
7	18	
8	17	08
9	16	07
10	15	06
11	14	05

ROM 8J
2Kx8
MASTER

A7	1	24	Vcc
A6	2	23	A8
A5	3	22	A9
A4	4	21	A10
A3	5	20	CS1
A2	6	19	CS2
A1	7	18	CS3
A0	8	17	08
01	9	16	07
02	10	15	06
03	11	14	05
GND	12	13	04

ROM 8J
2Kx8
SLAVE

	1	24	Vcc
	2	23	
	3	22	
	4	21	A10
	5	20	CS1
	6	19	CS2
	7	18	CS3
	8	17	08
01	9	16	07
02	10	15	06
03	11	14	05

ROM 8K
2Kx8
MASTER

A7	1	24	Vcc
A6	2	23	A8
A5	3	22	A9
A4	4	21	
A3	5	20	CS
A2	6	19	A10
A1	7	18	
A0	8	17	08
01	9	16	07
02	10	15	06
03	11	14	05
GND	12	13	04

ROM 8K
2Kx8
SLAVE

	1	24	Vcc
	2	23	
	3	22	
	4	21	
	5	20	CS
	6	19	A10
	7	18	
	8	17	08
01	9	16	07
02	10	15	06
03	11	14	05
GND	12	13	04

ROM 8L
32x8
MASTER

01	1	16	Vcc
02	2	15	CS
03	3	14	A4
04	4	13	A3
05	5	12	A2
06	6	11	A1
07	7	10	A0
GND	8	9	08

ROM 8L
32x8
SLAVE

01	1	16	Vcc
02	2	15	CS
03	3	14	
04	4	13	
05	5	12	
06	6	11	
07	7	10	
GND	8	9	08

ROM 8N
2Kx8
MASTER

A7	1	24	Vcc
A6	2	23	A8
A5	3	22	
A4	4	21	CS1
A3	5	20	CS2
A2	6	19	CS3
A1	7	18	CS4
A0	8	17	08
01	9	16	07
02	10	15	06
03	11	14	05
GND	12	13	04

A9,A10:AUX INPUT

ROM 8N
2Kx8
SLAVE

1	24	Vcc
2	23	
3	22	
4	21	CS
5	20	CS
6	19	CS
7	18	CS
8	17	08
9	16	07
10	15	06
11	14	05
12	13	04

01
02
03
GND

A10: AUX INPUT

ROM 8P
1Kx8
MASTER

A7	1	24	Vcc
A6	2	23	A8
A5	3	22	A9
A4	4	21	CS1
A3	5	20	CS2
A2	6	19	CS3
A1	7	18	
A0	8	17	08
01	9	16	07
02	10	15	06
03	11	14	05
GND	12	13	04

ROM 8P
1Kx8
SLAVE

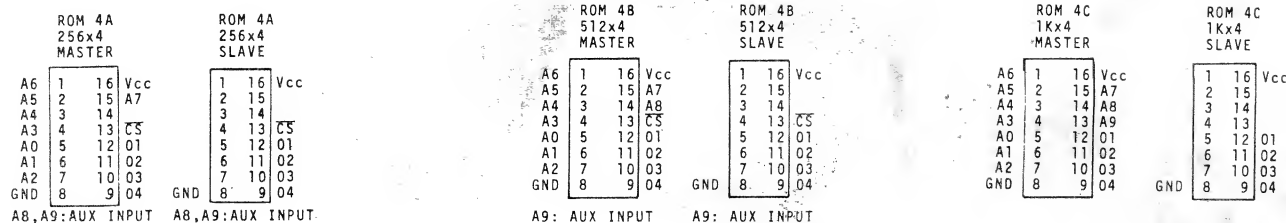
1	24	Vcc
2	23	
3	22	
4	21	CS1
5	20	CS2
6	19	CS3
7	18	
8	17	08
9	16	07
10	15	06
11	14	05
GND	12	13 04

Notes: A Output 01 is the Least Significant Bit, LSB.

B Each master module has two outputs, one master output and one slave. Each slave module has two slave outputs.

C This data sheet only shows a sample of ROM types offered. For more complete information, consult factory.

ROM-4 EMULATION



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Input Voltage	-1 to 5.5V
Output Current	150 ma
Storage Temp.	-45° to 75°C

Stresses above, and extended time at, absolute maximum rating may cause permanent damage or affect device reliability. Functional operation at these limits is not guaranteed or implied.

D.C. Characteristics (Ta=0 to 45° C^F; 4.75V ≤ V_{cc} ≤ 5.25V)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
"0" Input Current (CS only)	V _{in} = .50V			2	ma
"0" Input Current	V _{in} = .50V			-400	μa
"1" Input Current	V _{in} = 2.7V			50	μa
"0" Input Voltage		.85			V
"1" Input Voltage				2.0	V
"0" Output Voltage	I _{out} = 40 ma	.5			V
Output Short Circuit Current ^B	V _{out} = 0V			-30	ma
"1" Output Voltage	I _{out} = -6.5ma	2.4			V
Output Leakage Current				±50	μa
Input Clamp Voltage	I _{in} = 5.0ma			-1.0	V
Input Impedance (Address lines)			100		Ohms
Input Capacitance ^G	V _{in} = 2.0V		35		pf
Output Capacitance ^{D,E}	V _{in} = 2.0V		40		pf
Power Supply Current				200	ma

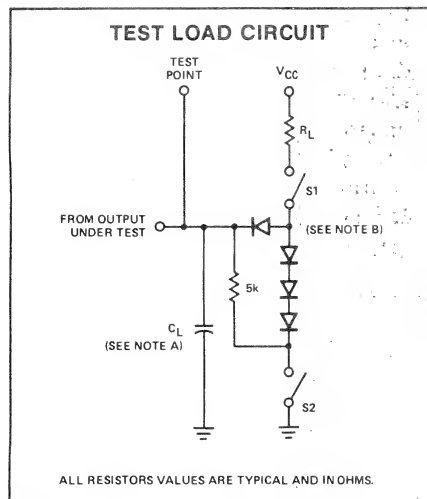
- Notes:
- A. Positive current is defined as into the terminal referenced.
 - B. No more than one output should be grounded at the same time.
 - C. Manufacturer reserves the right to make design and process changes and improvements.
 - D. All characteristics include the effect of the 12" cable between the buffer card and test signal.
 - E. Power off.
 - F. For high temperature operation to 125°C consult factory.
 - G. Input capacitance on slave address lines: 5pf typical.

AC Characteristics

SYMBOL	PARAMETER	VALUE	UNIT
T_{PHL}, T_{PLH}	Address Access Time ^A	$60 + 3.5/\text{cable ft.}$	nsec
T_{ZL}, T_{ZH}	Enable to output delay	25	nsec
T_{LZ}, T_{HZ}	Output disable time	20	nsec
T_W	Latch clock width ^B	20	nsec
T_S	Data setup time ^B	5	nsec
T_H	Data hold time ^B	15	nsec

- Notes:**
- A.** Worst case address to address transition utilizing a galloping pattern (GALPAT). Measured at DIP plug (includes memory access time).
 - B.** Numbers applicable to ROM-8A, ROM-8D and ROM-8P only and are referenced from negative edge of clock.

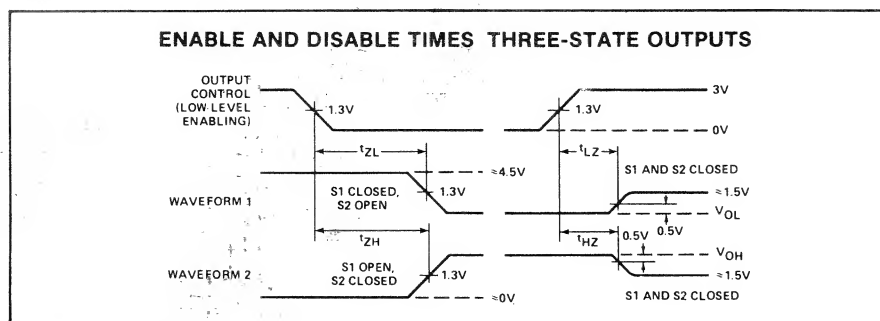
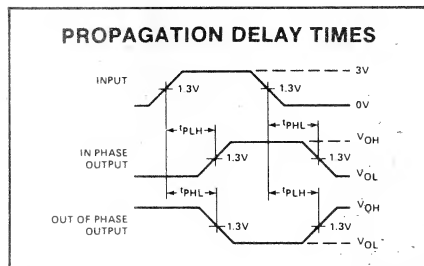
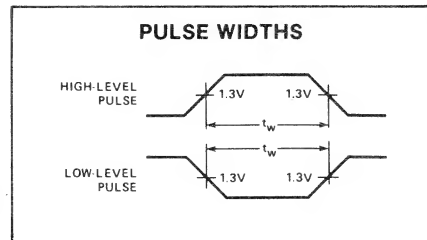
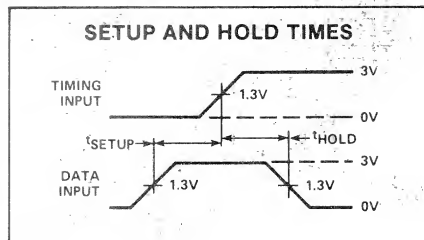
PARAMETER MEASUREMENT INFORMATION



NOTES

- A. C_L includes probe and jig capacitance.
- B. All diodes are 1N916 or 1N3064.
- C. $R_L = 2k$, $C = 15pF$.

VOLTAGE WAVEFORMS



New products

Trace cuts bit-slice firmware development time in half

The design of development tools and systems for MOS microprocessors has been awarded ample attention. But bit-slice and bipolar microprocessors need the same kind of support, and Step Engineering has been active in delivering it. Many development tools are already available via the Step-2 firmware integration and test system, including a writable control

New products

MON HLT ARR1 01KX32 SA=0000

SOURCE1 = 12

0 OR CR=NO CHANGE 1=RUN ALWAYS
2=TB1 3=TB2 4=TQ1 5=TQ2 6=UAC
7=TB1+TQ1 8=TQ1+TQ2 9=TB2+TQ2
10=TB1+TQ1+TQ2 11=TB1+TQ1+TQ2
12=TB1+TB2+TQ1

MON HLT ARR1 01KX32 SA=0000

RUN

B1=027F B2=NONE BR3=NONE

TRACE STATUS= ARMED
TRIG= TB1+TB2+TQ1 THEN 25 UAC

MON HLT ARR1 01KX32 SA=0000

238	D0D0	0001	1101	0000	0100
239	7171	0000	0110	0000	0000
240	F1F0	0001	1101	0000	0000
241	70F1	0010	1101	0000	0001
242	66D0	0100	0101	0000	0000

Trace. Menu (top) allows user to select trigger terms. Breakpoint equation (center) results in trace shown at bottom.

store for real-time emulation, diagnostic tools, a word-oriented editor, and loading and dumping programs. Now Step has taken the next step by adding a trace module that can cut firmware development time in half, over and above the savings already possible with the host instrument.

Tracing a bit-slice microprocessor's path of execution means following the address sequence of the machine and keeping a record of successive accesses to its microcoded control store, usually programmed into bipolar read-only memory. In real-time development work today, logic analyzers are usually called upon to do the tracing. The cost of the Step trace is one half to one third that of most logic analyzers.

Like the Step 2, the trace is optimized for bit-slice and bipolar devices such as 9405/10, 2900,

New products

8X300, 8X02, and S481. Also like the host, the trace is architecture-independent and will support MOS processors as well. Running at synchronous speeds up to 11 MHz, the trace allows the capture of 250 32-bit successive events (16 address bits and 16 data bits).

To set up the trace, the user selects from menus of trigger terms, as shown in the top photo. Choices include the breakpoint addresses, external qualifiers, and user address clocks, as well as combinations of these. The completed equation (bottom line in middle picture) takes many forms; here it uses breakpoint addresses shown in the fourth line of the display (027F₁₆). The resulting path of execution of the processor consists of line numbers (e.g., 238), addresses (e.g., D0D₁₆), and binary data collected by probes, as in the bottom photo.

The trace allows the actions of the microprocessor being designed to be tracked as the microcode is edited. And plain-English commands make the trace features quick to learn and easy to use. Available 75 days after receipt of order, the trace add-on costs \$2,750, complete with data and address cables.

Step Engineering, P. O. Box 61166, Sunnyvale, Calif. 94088

STEP ENGINEERING

PRELIMINARY DATA SHEET

FEATURES

- . FAST FAULT ISOLATION IN FIRMWARE CHECKOUT
- . SYNCHRONOUSLY CAPTURES:
 - 16 Address inputs
 - 16 User definable inputs
- . REAL TIME OPERATION (to 11 MHZ)
- . POWERFUL TRIGGERING MODES - TRACE INITIATED BY:
 - T Trigger: Address, qualifier, or clock
 - NT Nth trigger occurrence
 - C Trigger Combinations: AND, OR of address/qualifiers
 - C→NT Sequential trigger events:
 - NT→C Trigger event 1 followed by trigger event 2
- . CAPTURES 250 CYCLES BEFORE, AROUND, OR AFTER TRIGGER
- . EASY TRACE SETUP AND EXAMINATION
- . INSTALLS IN STEP-2 FIRMWARE INTEGRATION AND TEST STATION

DESCRIPTION

The Trace option provides a convenient means to follow the path of execution of the target processor. It simplifies fault isolation of firmware problems and greatly enhances the usefulness of STEP-2. Both address and data information are synchronously captured at rates up to 11 MHz without affecting target processor operation. An extensive triggering capability provides easy isolation of the program segment to be monitored. Setup of trace parameters is easy--the CRT prompts display all the choices, and the parameters can be examined or modified at any time. The "snapshot" captured is displayed on command in a convenient hex, octal or binary format on STEP-2s CRT.

INSTALLATION

The Trace option installs in the top slot of the STEP-2 backplane, leaving three slots available for memory boards. Connection to the target processor address bus is through the Master ROM SIMULATION ASSEMBLY. An additional external probe is used for the remaining upper order addresses, address clock, and external triggers. Two other external probes serve as inputs for sixteen data lines and the data clock. In all, 32 bits of information, 16 address and 16 data, are captured during each processor cycle. The probes connect into the target processor through clips, or slide directly onto square or round posts.

TRIGGERING

Finding firmware problems is simplified by the extensive triggering facility built into Trace. This facility permits easy specification of the program segment to be monitored. A trace can be initiated by a trigger, such as an address compare; by the Nth occurrence of the trigger; or by a trigger followed by a second independent trigger. Twelve equations ranging from simple qualifiers and address comparators to logical expressions specify the trigger sources. The trigger position within the captured data is also programmable, allowing events up to, around or after the trigger to be monitored.

The trigger flexibility makes possible the capture of complex data such as:

- the entrance/exit conditions from subroutine
- a subroutine the Nth time it is called
- processor activity N clocks after an event
- a routine after a control line has been set and an external event has occurred N times.

These capabilities, combined with the ability of STEP-2 to rapidly modify control-store memory, add a new dimension to firmware diagnosis.

Trigger setup is easy to learn and takes only seconds to accomplish. A series of "menus" display the current selection and options in the following sequence: First Trigger Event, Number of Events to Trigger (if applicable), Second Trigger Event, Number of Events to Trigger (if applicable), Trigger Position within captured data, Breakpoint Assignment. During the presentation of each option, the current selection is displayed. The new choice can be entered, or the old choice may be retained and the next menu called by hitting carriage return. At any time, the address-compare values can be modified to follow the processor's execution path, without changing the Trace Setup.

EVENT CAPTURE

Up to 250 processor cycles are synchronously captured during a Trace. Three separate references signals, or clocks, may be used for information capture: one for address and one for each of the two eight-bit data probes. The clock edge used to synchronously latch incoming addresses and data is individually switch programmable, negative or positive. An external enable line is provided to allow direct control over information to be captured. This allows a series of snapshots of processor activity or provides a way to lengthen the time span of Trace by capturing every Nth processor cycle.

TRIGGER EQUATIONS

#	EQN	MODE REF	DESCRIPTION
1	-	-	Always triggered
2	TB1	T, C	Trace Breakpoint 1 (16 Bit Address Comparator)
3	TB2	T, C	Trace Breakpoint 2 (16 Bit Address Comparator)
4	TQ1	T, C	Trace Qualifier 1
5	TQ2	T, C	Trace Qualifier 2
6	UAC	T, C	User Address Clock (From Target Processor)
7	TB1.TQ1	C	Logical "AND" of TB1, TQ1
8	TB2.TQ2	C	Logical "AND" of TB2, TQ2
9	TQ1.TQ2	C	Logical "AND" of TQ1, TQ2
10	TB1.TQ1.TQ2	C	Logical "AND" of TB1, TQ1, TQ2
11	TB1+TQ1+TQ2	C	Logical "OR" of TB1, TQ1, TQ2 Note: TB1+TQ1, TB1+TQ2, TQ1+TQ2 can be obtained using this specification
12	TB1+TB2+TQ1	C	Logical "OR" of TB1, TB2, TQ1 Note: TB1+TB2, TB1+TQ1, TB2+TQ1 can be obtained using this specification

TRIGGER EVENT NUMBER, N

The Trigger Event Number defines the number of times a "T" trigger input occurs before a trigger is generated. N=1 to 255

TRIGGER MODES

TRIGGER DEFINITION

C	Trace on the first occurrence of chosen combinatorial trigger equation.
NT	Trace on the Nth occurrence of trigger input.
C→T	Trace on the first occurrence of trigger T after the first occurrence of the combinatorial equation (C).
T→C	Trace on the first occurrence of the combinatorial equation (C) after the first occurrence of Trigger T.
NT→C	Trigger on the first occurrence of C after the Nth occurrence of T.
C→NT	Trigger on the Nth occurrence of T after the first occurrence of C.

TRACE OUTPUTS (Available on BNC Connectors at board edge)

TRACE TRIGGERED TGD

A positive true signal available 2 or 3 processor cycles (depending on trigger mode), plus 25 ns after a valid trigger condition has occurred. Indicated on the CRT, TGD can be used to trigger an external logic analyzer.

TRACE DONE TD

A negative true signal available 2 or 3 processor cycles (depending on trigger mode) plus 25 ns after a trace has been completed. Indicated on the CRT.

TRACE INPUTS

<u>SIGNAL NAME</u>	<u>INPUT FROM</u>	<u>SIGNAL DEFINITION</u>
A1 thru A9 (A10, A11) ⁶	Master ROM Assembly	Least significant address inputs
(A10, A11) ⁶	Address Probe	Address input
A12, thru A15	Address Probe	Most significant address input
UAC ¹	Address Probe	User address clock
EE ²	Address Probe	External enable to trace operation
TQ1 ^{2,3,5} TQ2 ^{2,3,5}	Address Probe	External Trigger inputs
DO thru D7	Data Probe 1 ⁵	Least significant external
UDC ¹	Data Probe 1 ⁵	User data clock
D8 thru D15 (UDC ^{1,4})	Data Probe 2 ⁵	Most significant external data inputs

- Notes: 1 Clock edge used to latch data, positive or negative, is individually switch programmable.
- 2 Logical true input level is individually switch programmable, positive or negative.
- 3 Clock input, UAC or UDC, used to strobe signal is individually selectable.
- 4 Used only to synchronously latch data; not used for internal timing.
- 5 Use of this input is optional; to run, Trace needs only UAC and the least significant addresses.
- 6 A10, A11 input can be obtained from either the Master ROM Assembly or Address Probe.

AC SPECIFICATIONS

Setup time from clock edge (ns)

	CLOCK EDGE				REFERENCE CLOCK
	NEGATIVE		POSITIVE		
	TYP	MIN	TYP	MIN	
Data	25	30	20	25	UDC
Address	25	35	20	30	UAC
EE	30	45	25	40	UAC and UDC

Minimum clock width (high or low: 25 ns)

Trace cycle time: 90 ns guaranteed, 80 ns typical

Specifications subject to change without notice.

STEP ENGINEERING

now 36 ns!

WRITABLE CONTROL STORE

FEATURES

- 32K bits high speed storage
- Switch selectable memory organization: 1K x 32, 2K x 16, 4K x 8
- Stackable to obtain word widths to 192 bits
- Real time operation
- User configurable interface
- Optional ROM emulator outputs
- Hardware bit mapping
- Integral real time breakpoint
- Read/Write operation
- 45 ns worst case access time, "A" version
- 36 ns worst case access time, "F" version

DESCRIPTION

General

MEM-32 is a dual-port, high-speed, 32K-bit Writable Control Store family that plugs into STEP-2 Firmware Integration and Test Station. One port is accessed from STEP-2 to load, dump, or modify memory contents. The second port is accessed by the user's system (target processor) in either a read only or read/write mode. MEM-32 replaces all or part of the target processor's ROM, PROM, and even RAM memory during system debug and/or test, permitting rapid changes to the code to find or patch microcode errors. MEM-32's 36 ns worst case access time allows the user's system to run at fast real time rates.

Memory Organization

Up to three MEM-32's can be plugged into a STEP-2 instrument giving the user a total of 96K bits of memory space. With the optional expansion chassis, an additional 96K bits of storage can be added for a total of 192K bits. Both MEM-32 and MEM-128 WCS can be resident in STEP-2 when assigned to different memory arrays. Each WCS is self-contained with its own address input, breakpoint output, and data output. The standard configuration is 1K x 32 but the

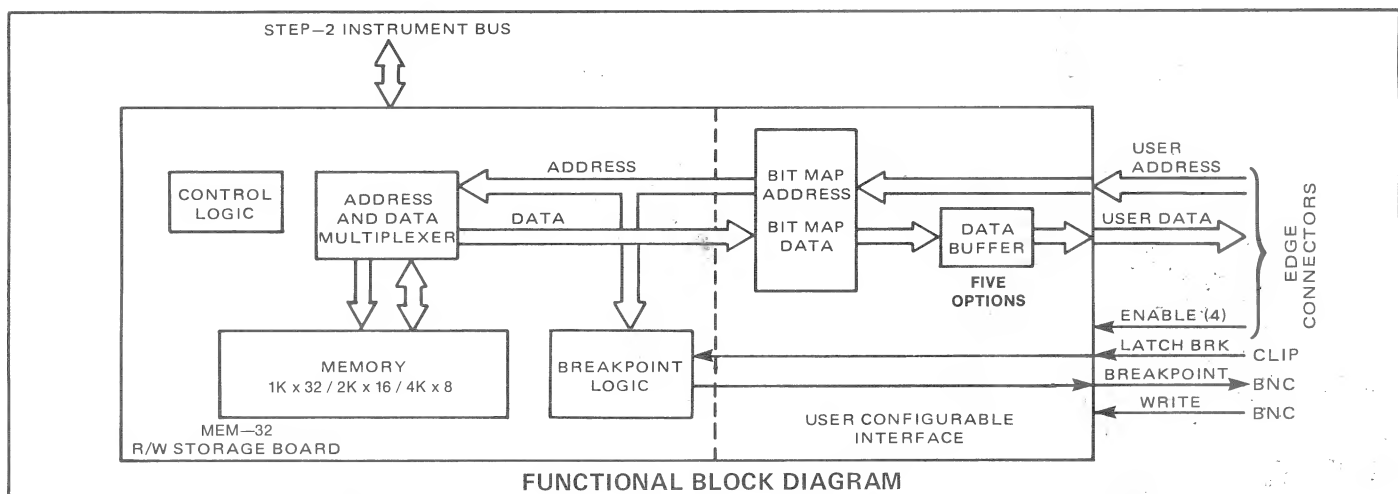
outputs can be OR'ed together to form a 2K x 16 array or a 4K x 8. Two or more Writable Control Stores can be combined creating either deeper or wider memory arrays. Word widths of 8, 16, 24, 32, 48, 64 or 96 bits (192 bits with expansion chassis) can be achieved.

Address Comparator

Each MEM-32 has an internal real-time address comparator which can generate a breakpoint to halt the target processor or serve as a trigger for another diagnostic instrument. A breakpoint display of each comparator's output state is provided on STEP-2's CRT. An optional qualifier input is provided to insure that only valid addresses are used as comparator inputs. The qualifier input is switch selectable: high or low true, edge or level sensitive.

Write Operation

The MEM-32 contains circuitry to allow its use as a read/write memory. A BNC connector is provided for the write-control input. When this input becomes low, the data output goes tristate, allowing input data to be written to the RAM. A switch is provided to inhibit write operation when the option is not desired.



CONFIGURABLE INTERFACE OPTIONS

- INT-1** Unbuffered output with 51-ohm series terminations for cable driving. The output should not be connected to more than one TTL load and cannot be wire-ORed. Used with ROM EMULATOR OUTPUTS to plug directly into system ROM sockets. (INT-1 is supplied as standard.)
- INT-2** Bidirectional buffered tristate output with outputs capable of wire-ORed configuration. Each group of eight bits has its own enable input. IC used: 74LS245. This is a special-order option.
- INT-3** Buffered tristate output with edge-triggered latches for direct use in pipeline organizations. IC used: 74S374.
- INT-4** Buffered tristate output with transparent latch. Outputs are capable of wire-ORed operation. IC used: 74S373.
- INT-5** Buffered tristate output without latch. Outputs are capable of wire-ORed operation. IC used: 74S373.
- ROM 4/8** Field-upgradable, plug-in ROM simulator cable assemblies that emulate over 200 bipolar ROMs and PROMs: See ROM 4/8 data sheet.

PINOUT^A OF MEM-32 BOARD EDGE

Conductor #	P10 ^{B,C}	P12 ^{D,E,F}	P11 ^{D,E,F}
1	A0	D0	D16
3	A1	D1	D17
5	A2	D2	D18
7	A3	D3	D19
9	A4	D4	D20
11	A5	D5	D21
13	A6	D6	D22
15	A7	D7	D23
17	A8	$\overline{E00}$	$\overline{E02}$
19	A9	$\overline{E10}$	$\overline{E12}$
21	A10	D8	D24
23	A11	D9	D25
25	UL	D10	D26
27	—	D11	D27
29	—	D12	D28
31	—	D13	D29
33	—	D14	D30
35	—	D15	D31
37	—	$\overline{E01}$	$\overline{E03}$
39	—	$\overline{E11}$	$\overline{E13}$

CONNECTOR TYPES

- READ/ $\overline{\text{WRITE}}$** — BNC Connector
- BREAKPOINT** — BNC Connector
- ADDRESS^G** — P10 26-conductor edge connector, 0.1" conductor spacing. Mating part 3M#3462-0001 or equivalent.
- MEMORY OUTPUTS^G** — P11, P12 Two 40-conductor edge connectors, 0.1" conductor spacing. Mating part 3M#3464-0001 or equivalent.

MEMORY ORGANIZATION (D0 IS LSB)

1K x 32	D0 through D7: Least Significant Byte D24 through D31: Most Significant Byte
2K x 16	D0 through D7: 0-1K Least Significant Byte D8 through D15: 1K-2K Least Significant Byte D16 through D23: 0-1K Most Significant Byte D24 through D31: 1K-2K Most Significant Byte
4K x 8	D1 through D7: 0-1K D8 through D15: 1K-2K D16 through D23: 2K-3K D24 through D31: 3K-4K

- Notes:
- A. Even-Numbered Pins: GND
 - B. UL = User Latch Input (Breakpoint Qualifier)
 - C. Ax = Address Input
 - D. Dx = Data Output
 - E. Elx = Enable Input (8 bits of data)
 - F. Elx = Enable Output (from STEP-2)
 - G. Connector cables supplied with unit. Standard terminations are 3M#3399 (Address) and two 3M#3421 (Data).
- } 0 = LS Bit
- } 0 = LS Byte

ELECTRICAL PARAMETERS

Absolute Maximum Ratings

Input Voltage	−1.5 to 5.5 V
Output Current	150 mA
Storage Temp.	−45° to 75°

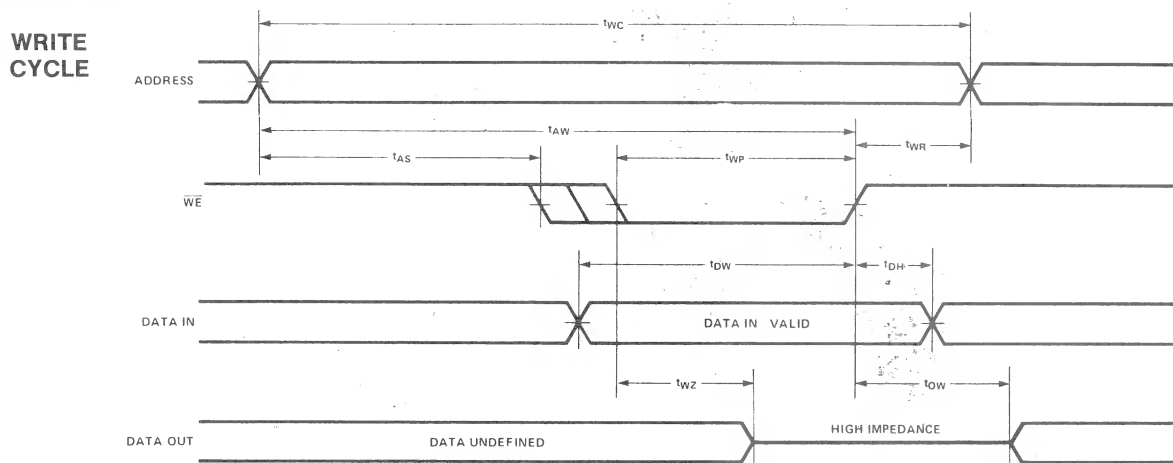
Stresses above, and extended time at, absolute maximum rating may cause permanent damage or affect device reliability. Functional operation at these limits is not guaranteed or implied.

DC Characteristics ($T_A = 0$ to 45°C)

Parameter	Test Conditions	INT-1		INT-2		INT-3,4,5		Units
		Min	Max	Min	Max	Min	Max	
ADDRESS & ENABLE LINES								
"0" Input Current	V _{IN} = 0.45 V		−400		−400		−400	μA
"1" Input Current	V _{IN} = 2.7 V		50		50		50	μA
"0" Input Voltage			0.8		0.8		0.8	V
"1" Input Voltage		2		2		2		V
Input Hysteresis		0.2		0.2		0.2		V
Input Clamp Voltage	I _{IN} = 18 mA		−1.5		−1.2		−1.2	V
DATA LINES								
"0" Output Voltage	I _{OUT} = 20 mA ^D		0.5		0.5		0.5	V
"1" Output Voltage	I _{OUT} = −6.5 mA ^D	2.4		2.4		2.4		V
Output Short Circuit Current ^B	V _{OUT} = 0 V		−30	−40	−225		−100	mA
Output Leakage Current	Tristate				+10		±50	μA
					−200			

- Notes:**
- A. Positive current defined as into terminal referenced.
 - B. No more than one output should be grounded at a time.
 - C. Manufacturer reserves the right to make design and process changes and improvements.
 - D. 1 mA for INT-1 interface, 3 mA for INT-2 interface.

AC Characteristics



WRITE CYCLE (Assumes Interface INT-1, Resistive Termination)

Symbol	Parameter	MEM-32F		MEM-32A		Unit
		Min	Max	Min	Max	
t_{WC}	Write Cycle Time	65		75		ns
t_{AW}	Address Valid to End of Write	55		65		ns
t_{AS}	Address Setup Time	10		10		ns
t_{WP}	Write Pulse Width	45		55		ns
t_{WR}	Write Recovery Time	15		20		ns
t_{DW}	Data Valid to End of Write	35		35		ns
t_{DH}	Data Hold Time	20		20		ns
t_{WZ}	Write Enabled to Output in High Z	0	35	20	35	ns
t_{OW}	Output Active from End of Write	20	40	25	40	ns

AC Characteristics (cont'd)

BREAKPOINT

	Min	Typ	Max	Unit
Address Input to Breakpoint Output		60	70	ns
Max Address Skew for "Glitchless Output"	4	6		ns

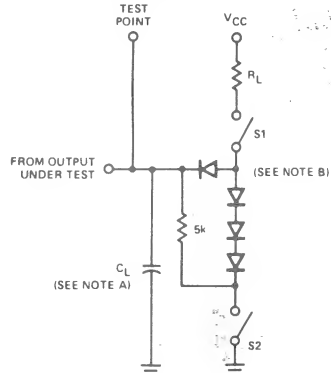
MEMORY READ

Symbol	Parameter	MEM TYPE	INT-1 Max	INT-2 Max	INT-3 ^C Min	INT-3 ^C Max	INT-4 ^D Min	INT-4 ^D Max	INT-5 Max	Unit
T _{PHL} , T _{PLH}	Address Access Time ^A	F	50	62		72		68	63	ns
T _{PHL} , T _{PLH}	Address Access Time ^A	A	70	82		92		88	83	ns
T _{PHL} , T _{PLH}	Address Access Time ^A	B	180	195		205		199	195	ns
T _{ZL} , T _{ZH}	Enable to Output Delay	all		40		25		25	25	ns
T _{HZ} , T _{LZ}	Output Disable Time	all		25		20		20		ns
T _W	Latch Clock Width	all			10		10			ns
T _S	Data Setup Time ^B	all			51		01			ns
T _H	Data Hold Time ^B	all			21		101			ns

- Notes:**
- A. Worst case address to data transition utilizing a galloping pattern (GALPAT).
 - B. Arrow indicates transition of latch input used for reference:
↑ for the low-to-high transition.
↓ for the high-to-low transition.
 - C. Access time includes data setups on register.
 - D. Worst case access: clock goes low after data sets up.

PARAMETER MEASUREMENT INFORMATION

TEST LOAD CIRCUIT

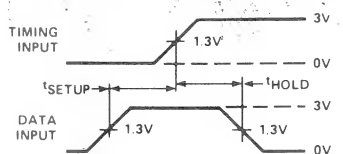


ALL RESISTORS VALUES ARE TYPICAL AND IN OHMS

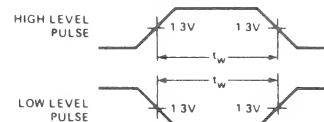
	INT-1	INT-2	INT-3,4,5
C _L	5	50	15
R _L	1K	90	280

VOLTAGE WAVEFORMS

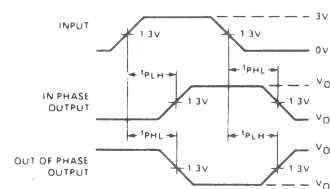
SETUP AND HOLD TIMES



PULSE WIDTHS



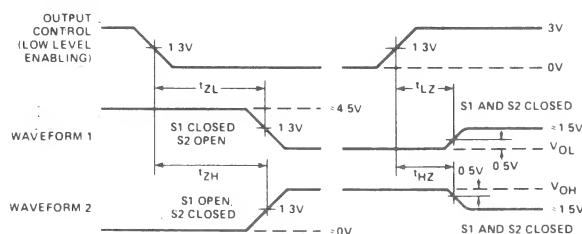
PROPAGATION DELAY TIMES



NOTES

- A. C_L includes probe and jig capacitance in pF.
- B. All diodes are 1N916 or 1N3064.

ENABLE AND DISABLE TIMES THREE-STATE OUTPUTS



STEP ENGINEERING

now 50 ns!

WRITABLE CONTROL STORE

FEATURES

- 128K bits high speed storage
- Switch selectable memory organization: 4K x 32, 8K x 16
- Stackable to obtain word widths to 192 bits
- Real time operation
- User configurable interface

DESCRIPTION

General

MEM-128 is a dual-port, high-speed, 128K-bit Writable Control Store family that plugs into STEP-2 Firmware Integration and Test Station. One port is accessed from STEP-2 to load, dump, or modify memory contents. The second port is accessed by the user's system (target processor) in either a read only or read/write mode. MEM-128 replaces all or part of the target processor's ROM, PROM, and even RAM memory during system debug and/or test, permitting rapid changes to the code to find or patch microcode errors. MEM-128F's 50 ns worst case access time and MEM-128A's 70 ns access allow the user's system to run at fast real time rates. An economical 180 ns (option "B") version of MEM-128 is also offered for slower systems or for use as main program memory.

Memory Organization

Up to three MEM-128's can be plugged into a STEP-2 instrument giving the user a total of 384K bits of memory space. With the optional expansion chassis, an additional 384K bits of storage can be added for a total of 768K bits. Both MEM-32 and MEM-128 WCS can be resident in STEP-2 when assigned to different memory arrays. Each WCS is self-contained with its own address input, breakpoint output, and data output. The standard configuration is 4K x 32 but

- Optional ROM emulator outputs
- Hardware bit mapping
- Integral real time breakpoint
- Read/Write operation
- 180 ns worst case access time, "B" version
- 70 ns worst case access time, "A" version
- 50 ns worst case access time, "F" version

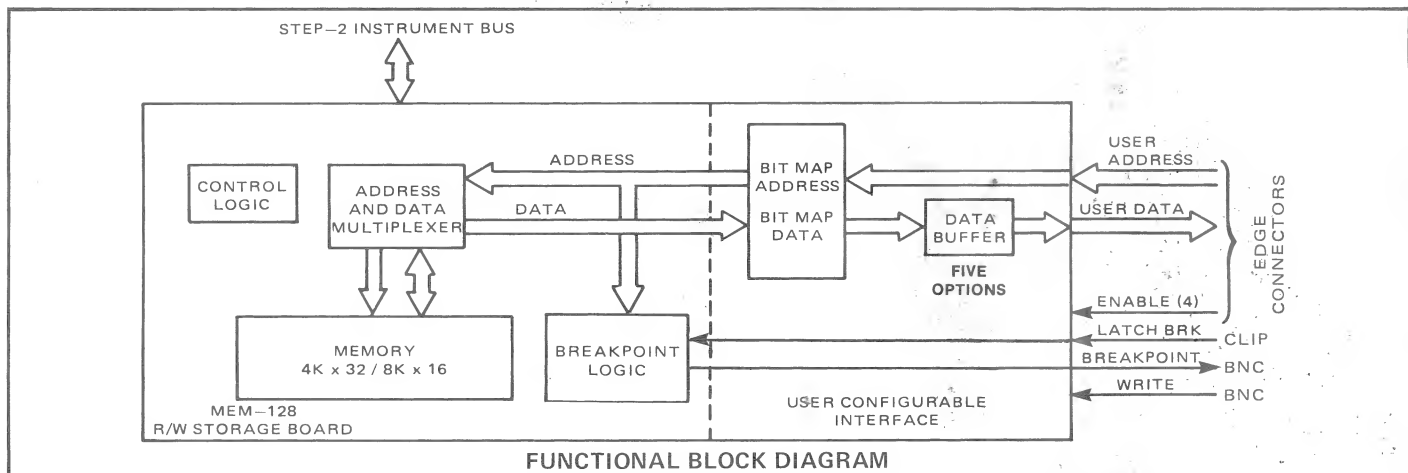
the outputs can be OR'ed together to form an 8K x 16 array. Two or more Writable Control Stores can be combined creating either deeper or wider memory arrays. Word widths of 16, 32, 48, 64 or 96 bits (192 bits with expansion chassis) can be achieved.

Address Comparator

Each MEM-128 has an internal real-time address comparator which can generate a breakpoint to halt the target processor or serve as a trigger for another diagnostic instrument. A breakpoint display of each comparator's output state is provided on STEP-2's CRT. An optional qualifier input is provided to insure that only valid addresses are used as comparator inputs. The qualifier input is switch selectable: high or low true, edge or level sensitive.

Write Operation

The MEM-128 contains circuitry to allow its use as a read/write memory. A BNC connector is provided for the write-control input. When this input becomes low, the data output goes tristate, allowing input data to be written to the RAM. Two switches are provided to inhibit write operation when the option is not desired. In the 8K x 16 organization, these switches permit writing into all or none of memory, or the upper 4K words only, or the lower 4K words only.



CONFIGURABLE INTERFACE OPTIONS

- INT-1** Unbuffered output with 51-ohm series terminations for cable driving. The output should not be connected to more than one TTL load and cannot be wire-ORed. Used with ROM EMULATOR OUTPUTS to plug directly into system ROM sockets. (INT-1 is supplied as standard.)
- INT-2** Bidirectional buffered tristate output with outputs capable of wire-ORed configuration. Each group of eight bits has its own enable input. IC used: 74LS245. This is a special-order option.
- INT-3** Buffered tristate output with edge-triggered latches for direct use in pipeline organizations. IC used: 74S374.
- INT-4** Buffered tristate output with transparent latch. Outputs are capable of wire-ORed operation. IC used: 74S373.
- INT-5** Buffered tristate output without latch. Outputs are capable of wire-ORed operation. IC used: 74S373.
- ROM 4/8** Field-upgradable, plug-in ROM simulator cable assemblies that emulate over 200 bipolar ROMs and PROMs: See ROM 4/8 data sheet.

CONNECTOR TYPES

- READ/WRITE** — BNC Connector
- BREAKPOINT** — BNC Connector
- ADDRESS^G** — P10 26-conductor edge connector, 0.1" conductor spacing. Mating part 3M#3462-0001 or equivalent.
- MEMORY OUTPUTS^G** — P11, P12 Two 40-conductor edge connectors, 0.1" conductor spacing. Mating part 3M#3464-0001 or equivalent.

PINOUT^A OF MEM-128 BOARD EDGE

Conductor #	P10 ^{B,C}	P12 ^{D,E,F}	P11 ^{D,E,F}
1	A0	D0	D16
3	A1	D1	D17
5	A2	D2	D18
7	A3	D3	D19
9	A4	D4	D20
11	A5	D5	D21
13	A6	D6	D22
15	A7	D7	D23
17	A8	$\overline{E00}$	$\overline{E02}$
19	A9	$\overline{E10}$	$\overline{E12}$
21	A10	D8	D24
23	A11	D9	D25
25	UL	D10	D26
27	—	D11	D27
29	—	D12	D28
31	—	D13	D29
33	—	D14	D30
35	—	D15	D31
37	—	$\overline{E01}$	$\overline{E03}$
39	—	$\overline{E11}$	$\overline{E13}$

MEMORY ORGANIZATION (D0 IS LSB)

- 4K x 32 D0 through D7: Least Significant Byte
D24 through D31: Most Significant Byte
- 8K x 16 D0 through D7: 0-4K Least Significant Byte
D8 through D15: 4K-8K Least Significant Byte
D16 through D23: 0-4K Most Significant Byte
D24 through D31: 4K-8K Most Significant Byte

- Notes: A. Even-Numbered Pins: GND
- B. UL = User Latch Input (Breakpoint Qualifier)
- C. Ax = Address Input } 0 = LS Bit
- D. Dx = Data Output }
- E. Elx = Enable Input (8 bits of data) } 0 = LS Byte
- F. Elx = Enable Output (from STEP-2) }
- G. Connector cables supplied with unit. Standard terminations are 3M#3399 (Address) and two 3M#3421 (Data)

ELECTRICAL PARAMETERS

Absolute Maximum Ratings

Input Voltage	-1.5 to 5.5 V
Output Current	150 mA
Storage Temp.	-45° to 75°

Stresses above, and extended time at, absolute maximum rating may cause permanent damage or affect device reliability. Functional operation at these limits is not guaranteed or implied.

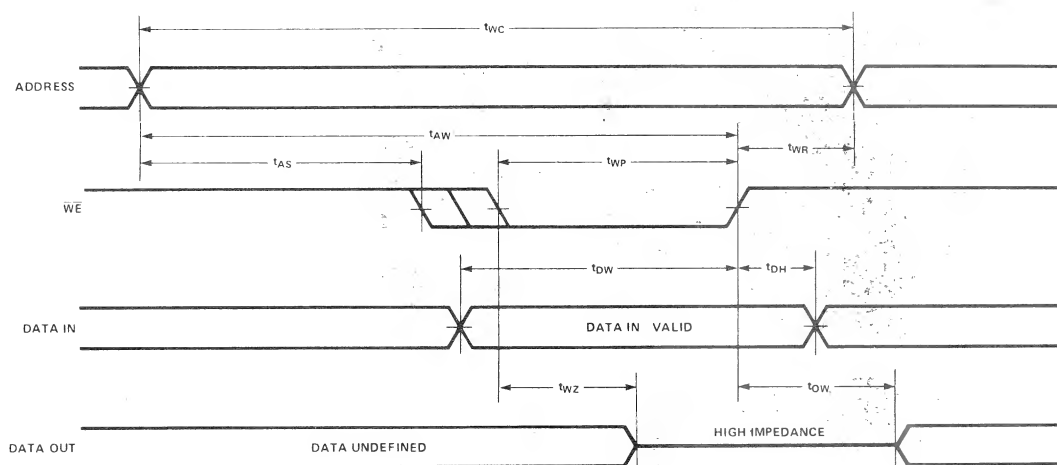
DC Characteristics ($T_A = 0$ to 45°C)

Parameter	Test Conditions	INT-1		INT-2		INT-3,4,5		Units
		Min	Max	Min	Max	Min	Max	
ADDRESS & ENABLE LINES								
"0" Input Current	V _{IN} = 0.45 V		−400		−400		−400	μA
"1" Input Current	V _{IN} = 2.7 V		50		50		50	μA
"0" Input Voltage			0.8		0.8		0.8	V
"1" Input Voltage		2		2		2		V
Input Hysteresis		0.2		0.2		0.2		V
Input Clamp Voltage	I _{IN} = 18 mA		−1.5		−1.2		−1.2	V
DATA LINES								
"0" Output Voltage	I _{OUT} = 20 mA ^D		0.5		0.5		0.5	V
"1" Output Voltage	I _{OUT} = −6.5 mA ^D	2.4		2.4		2.4		V
Output Short Circuit Current ^B	V _{OUT} = 0 V		−30	−40	−225		−100	mA
Output Leakage Current	Tristate				+10 −200		±50	μA

- Notes:**
- A. Positive current defined as into terminal referenced.
 - B. No more than one output should be grounded at a time.
 - C. Manufacturer reserves the right to make design and process changes and improvements.
 - D. 1 mA for INT-1 interface, 3 mA for INT-2 interface.

AC Characteristics

WRITE CYCLE



WRITE CYCLE (Assumes Interface INT-1, Resistive Termination)

Symbol	Parameter	MEM-128F		MEM-128A		MEM-128B		Unit
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	75		90		180		ns
t_{AW}	Address Valid to End of Write	40		50		155		ns
t_{AS}	Address Setup Time	10		10		20		ns
t_{WP}	Write Pulse Width	55		70		150		ns
t_{WR}	Write Recovery Time	10		20		15		ns
t_{DW}	Data Valid to End of Write	30		30		60		ns
t_{DH}	Data Hold Time	20		20		15		ns
t_{WZ}	Write Enabled to Output in High Z	0	30	0	40	10	85	ns
t_{OW}	Output Active from End of Write	5		5		5		ns

AC Characteristics (cont'd)

BREAKPOINT

	Min	Typ	Max	Unit
Address Input to Breakpoint Output		60	70	ns
Max Address Skew for "Glitchless Output"	4	6		ns

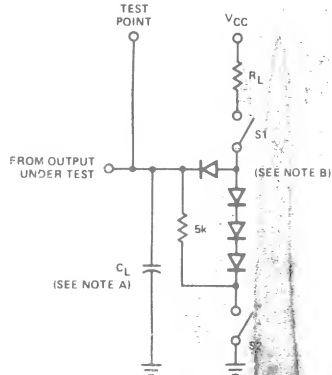
MEMORY READ

Symbol	Parameter	MEM TYPE	INT-1 Max	INT-2 Max	INT-3 ^C Min	INT-3 ^C Max	INT-4 ^D Min	INT-4 ^D Max	INT-5 Max	Unit
T _{PHL} , T _{PLH}	Address Access Time ^A	F	36	48		58		54	49	ns
T _{PHL} , T _{PLH}	Address Access Time ^A	A	45	57		67		63	58	ns
T _{ZL} , T _{ZH}	Enable to Output Delay	all		40		25		25	25	ns
T _{HZ} , T _{LZ}	Output Disable Time	all		25		20		20		ns
T _W	Latch Clock Width	all			10		10			ns
T _S	Data Setup Time ^B	all			51		01			ns
T _H	Data Hold Time ^B	all			21		101			ns

- Notes:**
- A. Worst case address to data transition utilizing a galloping pattern (GALPAT).
 - B. Arrow indicates transition of latch input used for reference:
↑ for the low-to-high transition.
↓ for the high-to-low transition.
 - C. Access time includes data setup time on register.
 - D. Worst case access: clock goes low after data sets up.

PARAMETER MEASUREMENT INFORMATION

TEST LOAD CIRCUIT

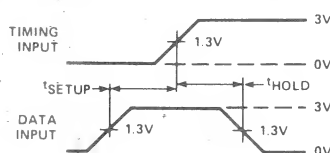


ALL RESISTOR VALUES ARE TYPICAL AND IN OHMS

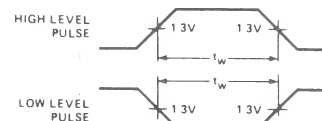
	INT-1	INT-2	INT-3,4,5
C _L	5	50	15
R _L	1K	90	280

VOLTAGE WAVEFORMS

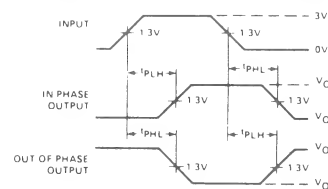
SETUP AND HOLD TIMES



PULSE WIDTHS



PROPAGATION DELAY TIMES



NOTES

- A. C_L includes probe and jig capacitance in pF.
- B. All diodes are 1N916 or 1N3064.

ENABLE AND DISABLE TIMES THREE-STATE OUTPUTS

